PATENT NUMBER and ISSUE DATE

U.S. **UTILITY** Patent Application

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10084789	02 25 2002	327		2816	

**APPLICANTS: Endo Masaki

**CONTINUING DATA VERIFIED:

** FOREIGN APPLICATIONS VERIFIED:
JAPAN P2001 050433 02/26/2001

PG-PUB | DO NOT PUBLISH ☐ | RESCIND ☐

Foreign priority claimed ☐ yes ☐ no
35 USC 119 conditions met ☐ yes ☐ no
Verified and Acknowledged Examiner's Initials

ATTORNEY DOCKET NO
450100-03853

TITLE : Delay lock loop circuit, varable delay circuit, and recording signal compensating circuit

NOTICE OF ALLOWANCE MAILED		Assistant Examiner	CLAIMS ALLOWED	
			Total Claims	Print Claim for O.G
ISSUE FEE			DRAWING		
Amount Due	Date Paid		Sheets Drwg.	Figs.Drwg.	Print Fig.
		Primary Examiner			
☐ TERMINAL DISCLAMER		PREPARED FOR ISSUE	Application Examiner		

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